A 3-BIT GaAs ANALOG-TO-DIGITAL CONVERTER

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ABSTRACT

A 3-bit GaAs analog-to-digital converter (ADC) using a parallel architecture has been designed and fabricated. A latched regenerative comparator design approach is used. Depletion mode MESFET technology was used for circuit implementation. Successful functionality tests of the comparator and the ADC have been completed on the first circuits. These show that comparator offset uniformity needs to be improved. High-speed tests will be underway shortly with results to be presented at the conference.

INTRODUCTION

High speed analog-to-digital converters are important components in many high performance electronic systems. GaAs analog-to-digital converters (ADCs) have the potential for higher conversion speed than Si ADCs of equal complexity. In this paper we describe our initial work whose objective was to identify the important problem areas and to determine the level of ADC complexity that can be readily achieved with the use of existing technology.

DESIGN

Figure 1 shows the schematic for a 3-bit analog-to-digital converter which uses a parallel or flash architecture. For simplicity, the clocks to the comparators are not shown. Circuit operation will now be illustrated by example. Suppose the analog signal at a particular instant is greater than the reference voltage to C_5 but less than the reference voltage to C_6. In that event, the Q outputs of C_5 through C_1 are high while those of C_6 through C_7 are low. Using the complementary outputs together with AND gates as shown by the schematic, a "peak detector" of the input "thermometer scale" is constructed; that is, only node 5 is high. Encoders are then used to convert the single output to binary form; that is, the "5" is converted to "101". D-type latches are then used to strobe the encoder outputs; the latch clock being referenced to the comparator clock. The microphotograph of Fig. 2 is the physical realization of the circuit schematically represented by Fig. 1.

Conventional processing techniques were used to fabricate the circuit [1]. Not-intentionally doped GaAs substrates grown by the liquid encapsulated Czochralski method were selectively ion-implanted with Si and the wafer subsequently annealed at 850°C to create an active region doped to about 1.7×10^{17} cm^{-3}. Device isolation was enhanced by using a boron implant to damage the region between devices and thereby reduce backgating effects. Ohmic contacts were formed by alloying the standard AuGeNi metallization into the surface. The nominally 1 micron gates are recessed about 75 nm to result in MESFET transconductances of about 135 mS/mm. Thereafter, two levels of metallization, separated by a polyimide dielectric, are used to interconnect the devices and complete the circuit.

The schematic of the latched regenerative comparator used for the ADC is shown by Fig. 3. This circuit is the MESFET equivalent to a bipolar circuit frequently used in silicon ADC circuits [2]. Hysteresis effects in this circuit are eliminated, in principal, by switching between an amplify mode and a latch mode. In the amplify mode there is no positive feedback and the output tracks the input. In the latch mode, regeneration causes the output to latch either high or low depending on the polarity of the differential signal at the Q and $\overline{Q}$ outputs. The microphotograph shown by Fig. 4 is the physical realization of the regenerative comparator schematically represented by Fig. 3. Although the comparator offset voltage is dependent on the layout of matched transistor pair Q_1 and Q_2 and their associated load resistors, in this first design attempt, no special effort was made to minimize the offset voltage by spatial averaging layout techniques of the matched transistor pairs [3].

CH2191-5/85/0000-0018 $1.00 © 1985 IEEE

TEST RESULTS

Functionality test results of the latched regenerative comparator is shown by Fig. 5. The photograph at the bottom shows details of comparator operation in the vicinity of V_{IN} equal to V_{Ref}. Correct operation is observed. When CLK is low, the comparator is in the amplify mode. When CLK is high, regeneration causes the output, as expected, to latch either high or low. For this particular comparator, the offset error is seen to be less than 100 mV which is typical. A differential signal input of less than +/- 50 mV is usually sufficient to cause the output to be latched into one of the binary states when the CLK (latch) goes high.

Figure 6 shows the response of the ADC when a triangular waveform is applied to the analog input. Correct circuit operation is demonstrated by Fig. 6(a). The relationship of the comparator clocks and the D-latch clock to the bit pattern is shown by Fig. 6(b). Although the sampling rate is not very much greater than the frequency of the LSB, it is nonetheless clear from these photographs that comparator offset uniformity needs to be improved.

High-speed evaluation of the ADC will be undertaken with the use of a 4-bit digital-to-analog converter (DAC) located in close proximity to the ADC. (The DAC is at upper right in the microphotograph of Fig. 2). Although such testing has not yet been completed satisfactorily, simulations suggest that ADC operation with clocks approaching 2 GHz should be possible.

CONCLUSIONS

Assuming an analog input signal having a 1.6 V peak-to-peak amplitude, our preliminary conclusions from this work can be summarized as follows:

- Three-bit analog-to-digital converters can be constructed as described by this paper.
- Four-bit and 5-bit ADCs can probably be achieved by 1-dimensional and 2-dimensional spatial averaging layout techniques of the matched transistor pairs, respectively. Thin film resistors will most probably be required.
- To achieve 6-bit resolution, either resistor trimming or the use of dislocation-free GaAs substrates in conjunction with 2-dimensional spatial averaging techniques will most probably be necessary.

ACKNOWLEDGEMENTS

The authors thank N.R. Miner for technical assistance in circuit fabrication.

REFERENCES

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[2] M.R. Namordi, W.A. White, W.M. Duncan, and C.T.M. Chang, "Planar High Speed GaAs Technology", Final Technical Report AFWAL-TR-83-1153, November 1983.

[3] P. Greiling, et al., "GaAs Technology for High Speed A/D Converters", 1984 GaAs IC Symposium Technical Digest, p. 31.

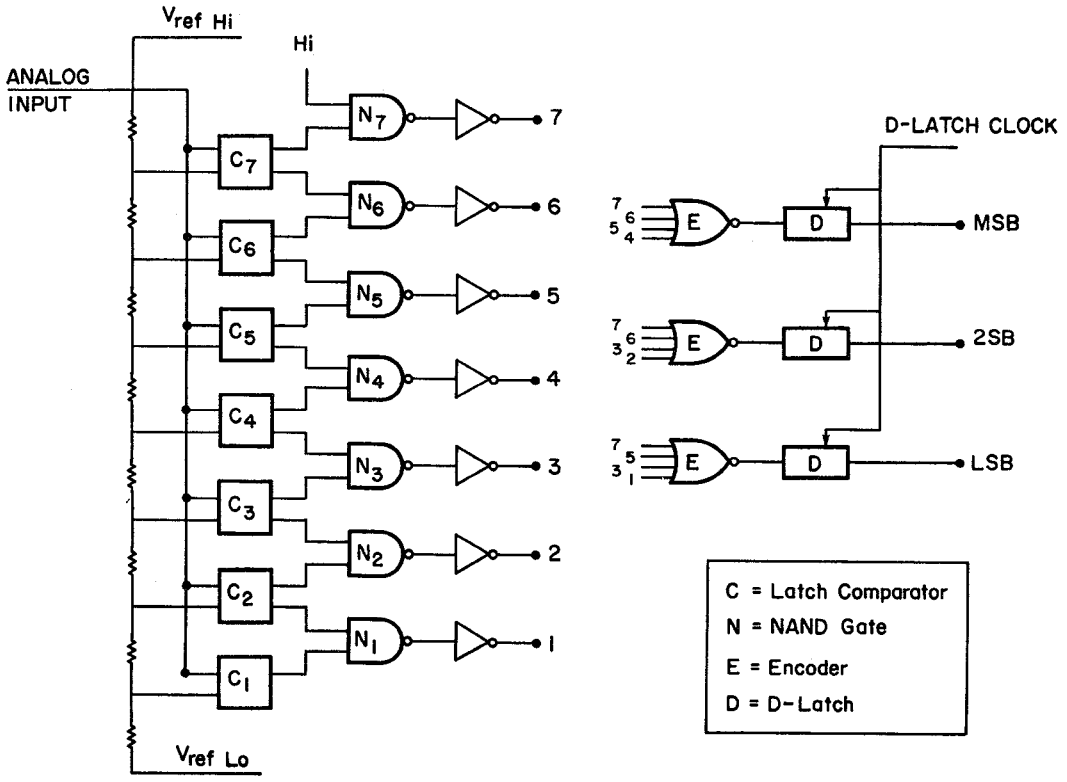

Figure 1. Three-bit analog-to-digital converter: Flash architecture.

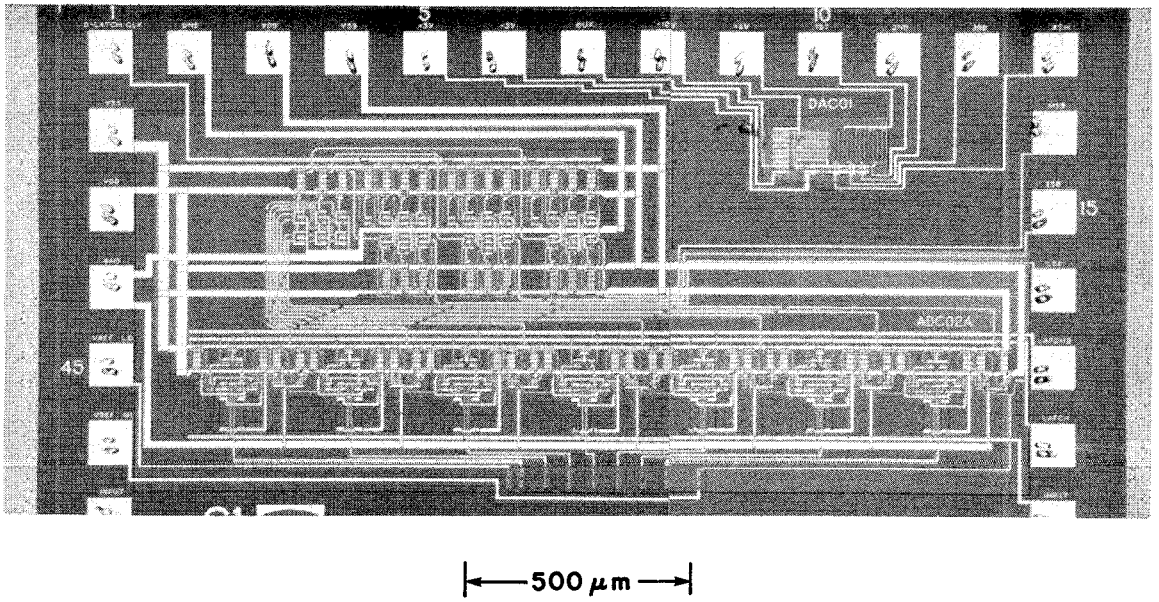

Figure 2. Physical realization of 3-bit analog-to-digital converter.

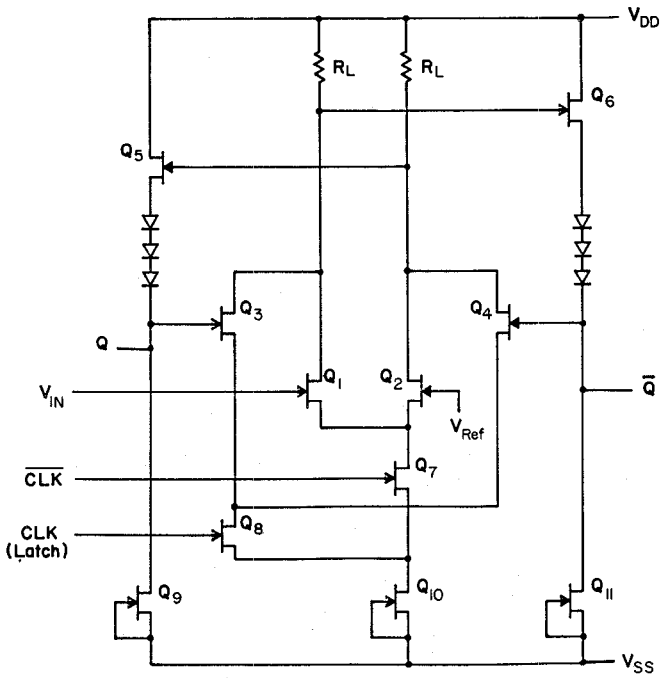

Figure 3. Schematic of a latched regenerative comparator.

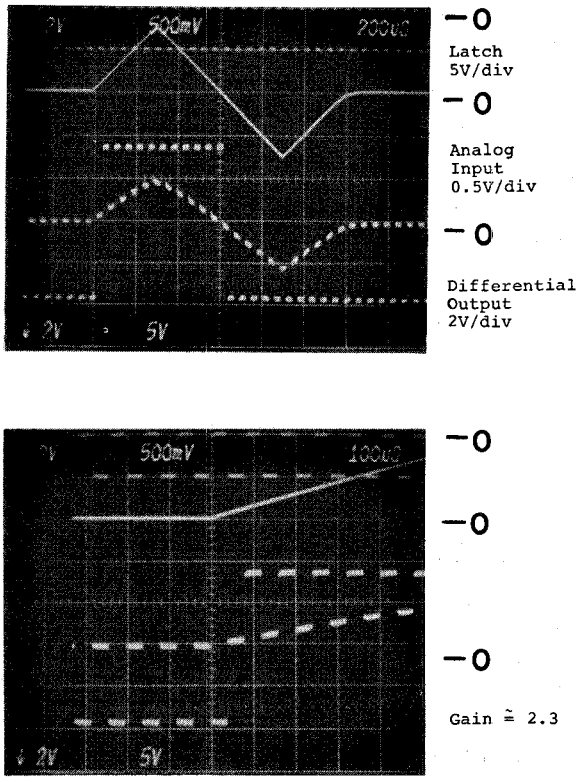

Figure 5. Response of a GaAs MESFET latched regenerative comparator.

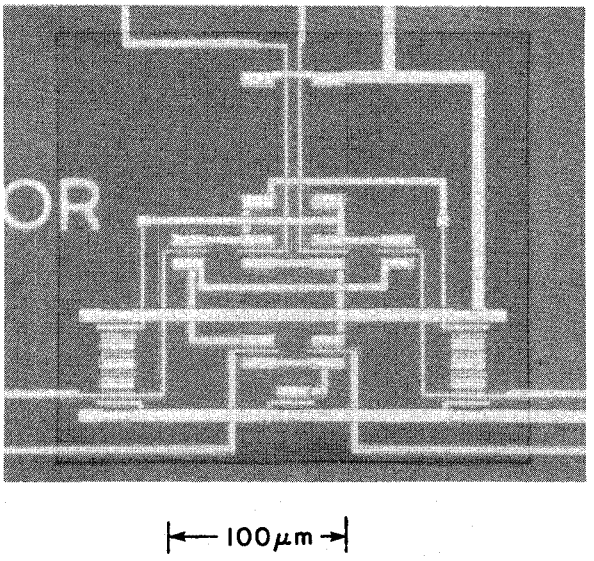

Figure 4. Layout of latched regenerative comparator.

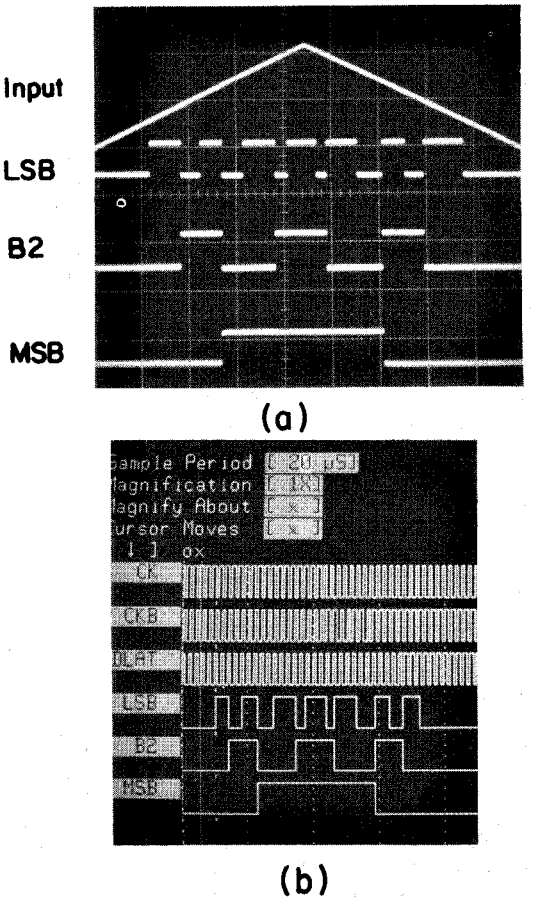

Figure 6. Response of 3-bit ADC to a triangular wave input. Vertical: Input = 2 V/div. Output bits = 5 V/div.